

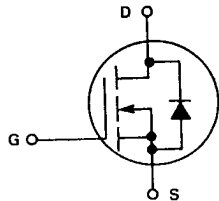
MOTOROLA SEMICONDUCTOR TECHNICAL DATA

**IRF510
IRF511
IRF512
IRF513**

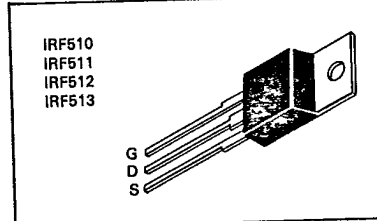
N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



Part Number	V _{DS}	r _{DS(on)}	I _D
IRF510	100 V	0.6 Ω	4.0 A
IRF511	60 V	0.6 Ω	4.0 A
IRF512	100 V	0.8 Ω	3.5 A
IRF513	60 V	0.8 Ω	3.5 A



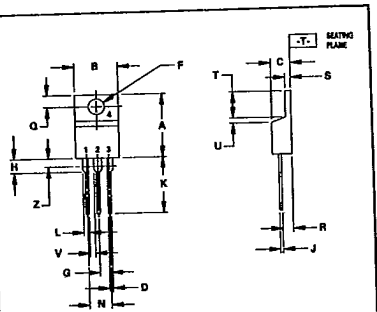
MAXIMUM RATINGS

Rating	Symbol	IRF				Unit
		510	511	512	513	
Drain-Source Voltage	V _{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V _{GS}	± 20				Vdc
Continuous Drain Current T _C = 25°C	I _D	4.0	4.0	3.5	3.5	Adc
Continuous Drain Current T _C = 100°C	I _D	2.5	2.5	2.0	2.0	Adc
Drain Current Pulsed	I _{DM}	16	16	14	14	Adc
Total Power Dissipation @ T _C = 25°C	P _D	20				Watts
Derate above 25°C		0.16				W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	R _{θJC}	6.4	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T _L	300	°C

See the MTP6N10 Designer's Data Sheet for a complete set of design curves for this product.



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
- STYLE 5:
 PIN 1 GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.45	15.75	0.571	0.620
B	9.68	10.28	0.381	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.98	0.025	0.039
F	3.81	3.73	0.142	0.147
G	2.42	2.66	0.095	0.106
H	2.80	3.93	0.110	0.155
J	0.26	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.29	0.045	0.051
M	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.92	1.27	0.036	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA TMOS POWER MOSFET DATA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 250 \mu\text{A}$)	$V_{(BR)DSS}$	100 60	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0 \text{ V}, V_{DS} = \text{Rated } V_{DSS}$) ($V_{GS} = 0 \text{ V}, V_{DS} = 0.8 \text{ Rated } V_{DSS}, T_C = 125^\circ\text{C}$)	I_{DSS}	—	—	0.25 1.0	mAdc
Forward Gate-Body Leakage Current ($V_{GS} = 20 \text{ V}, V_{DS} = 0$)	I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current ($V_{GS} = -20 \text{ V}, V_{DS} = 0$)	I_{GSSR}	—	—	-100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$)	$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current ($V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V}$)	$I_{D(on)}$	4.0 3.5	—	—	Adc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ V}, I_D = 2.0 \text{ A}$)	$r_{DS(on)}$	—	—	0.6 0.8	Ohms
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_D = 2.0 \text{ A}$)	g_{FS}	1.0	—	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{iss}	—	—	150	pF
Output Capacitance	C_{oss}	—	—	100	
Reverse Transfer Capacitance	C_{rss}	—	—	25	

($V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Turn-On Delay Time	$t_{d(on)}$	—	—	20	ns
Rise Time	t_r	—	—	25	
Turn-Off Delay Time	$t_{d(off)}$	—	—	25	
Fall Time	t_f	—	—	20	

$V_{DD} = 0.5 V_{DSS}, I_D = 2.0 \text{ A}$
 $Z_o = 50 \Omega$

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Symbol	Typ	Unit
Forward On-Voltage	V_{SD}	2.0	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance	
Reverse Recovery Time	t_{rr}	230	ns

($I_S = \text{Rated } I_D, V_{GS} = 0$)

INTERNAL PACKAGE INDUCTANCE (TO-220)

Characteristic	Symbol	Min	Typ	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	—	7.5	—	

*Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

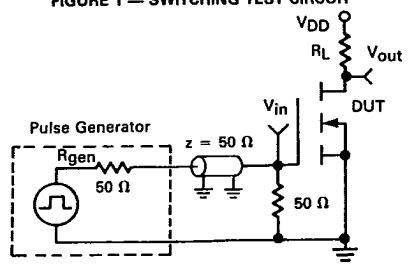


FIGURE 2 — SWITCHING WAVEFORMS

